Notice of Allowability	Application No.	Applicant(s)
	10/717,155	TUNG, KE-WEI
	Examin r	Art Unit
	Jack Chen	2813
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.		
1. This communication is responsive to <u>5/5/04.</u>		
2. ☑ The allowed claim(s) is/are <u>1-16</u> .		
3. 🔀 The drawings filed on 19 November 2003 are accepted by the Examiner.		
 4. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a)		
 Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 11/19/03 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material 	6. Interview Summary Paper No./Mail Da 7. Examiner's Amend	ate

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DETAILED ACTION

Reasons For Allowance

1. Claims 1-16 are allowable over the prior art of record.

2. The following is an examiner's statement of reasons for allowance: the prior art of record neither teach nor make obvious the claimed limitation of the instant application as a whole as recited in claims 1 and 8 respectively. In particular, the prior art does not teach or suggest the particular subset of the process steps for forming non-volatile memory device by filling a second sacrificial layer in the opening of the first sacrificial layer; patterning the first patterned sacrificial layer and the insulating composite layer (i.e., the second dielectric layer and the charge-trapping layer) by using the second sacrificial layer as masks and exposing the dielectric layer (i.e., the tunnel dielectric layer); removing the second sacrificial layer and forming control gate on the composite layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Wang et al.; Chang et al.; Lai and Liu et al. Disclose the similar processes for forming the memory device; however; these references at least fail to shown the above-cited steps.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jack Chen

Sarel

Primary Examiner

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